



**ARM Cortex™-M0**  
**32-BIT MICROCONTROLLER**

**NuMicro™ Family**  
**M058/M0516BN Product Brief**



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## 1 GENERAL DESCRIPTION

The NuMicro M051™ series is a 32-bit microcontroller with embedded ARM® Cortex™-M0 core for industrial control and applications which need rich communication interfaces. The Cortex™-M0 is the newest ARM embedded processor with 32-bit performance and at a cost equivalent to traditional 8-bit microcontroller. The NuMicro M051™ series includes M052, M054, M058 and M0516 families.

The M058/M0516 can run up to 50 MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. The M058/M0516 has 32K/64K-byte embedded flash, 4K-byte data flash, 4K-byte flash for the ISP, and 4K-byte embedded SRAM.

Many system level peripheral functions, such as I/O Port, EBI (External Bus Interface), Timer, UART, SPI, I2C, PWM, ADC, Watchdog Timer and Brownout Detector, have been incorporated into the M058/M0516 in order to reduce component count, board space and system cost. These useful functions make the M058/M0516 powerful for a wide range of applications.

Additionally, the M058/M0516 is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.



## 2 FEATURES

- Core
  - ARM® Cortex™-M0 core runs up to 50 MHz.
  - One 24-bit system timer.
  - Supports low power sleep-mode.
  - A single-cycle 32-bit hardware multiplier.
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority.
  - Supports Serial Wire Debug (SWD) interface and 2 watchpoints/4 breakpoints.
- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Memory
  - 32KB/64KB Flash memory for program memory (APROM)
  - 4KB Flash memory for data memory (DataFlash)
  - 4KB Flash memory for loader (LDROM)
  - 4KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
  - 4~24 MHz external crystal input
  - 22.1184 MHz internal oscillator (trimmed to 3% accuracy)
  - 10 kHz low-power oscillator for Watchdog Timer and wake-up in sleep mode
  - PLL allows CPU operation up to the maximum 50MHz
- I/O Port
  - Up to 40 general-purpose I/O (GPIO) pins for LQFP-48 package
  - Four I/O modes:
    - ◆ Quasi bi-direction
    - ◆ Push-Pull output



- ◆ Open-Drain output
- ◆ Input only with high impedance
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports high driver and high sink IO mode
- Timer
  - Provides four channel 32-bit timers, one 8-bit pre-scale counter with 24-bit up-timer for each timer.
  - Independent clock source for each timer.
  - 24-bit timer value is readable through TDR (Timer Data Register)
  - Provides one-shot, periodic and toggle operation modes.
  - Provide event counter function.
  - Provide external capture/reset counter function equivalent to 8051 Timer2.
- Watchdog Timer
  - Multiple clock sources
  - Supports wake up from power down or sleep mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Built-in up to four 16-bit PWM generators; providing eight PWM outputs or four complementary paired PWM outputs
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
  - PWM interrupt synchronized to PWM period
  - 16-bit digital Capture timers (shared with PWM timers) with rising/falling capture inputs
  - Supports capture interrupt
- UART



- Up to two sets of UART device
- Programmable baud-rate generator
- Buffered receiver and transmitter, each with 15 bytes FIFO
- Optional flow control function (CTS and RTS)
- Supports IrDA(SIR) function
- Supports RS485 function
- Supports LIN function
- SPI
  - Up to two sets of SPI device.
  - Supports master/slave mode
  - Full duplex synchronous serial data transfer
  - Provide 3 wire function
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx latching data can be either at rising edge or at falling edge of serial clock
  - Tx sending data can be either at rising edge or at falling edge of serial clock
  - Supports Byte suspend mode in 32-bit transmission
- I<sup>2</sup>C
  - Supports master/slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master).
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.



- Programmable clocks allow versatile rate control.
- Supports multiple address recognition (four slave address with mask option)
- ADC
  - 12-bit SAR ADC with 760k SPS
  - Up to 8-ch single-ended input or 4-ch differential input
  - Supports single mode/burst mode/single-cycle scan mode/continuous scan mode
  - Supports 2' complement/un-signed format in differential mode conversion result
  - Each channel with an individual result register
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
  - Conversion can be started either by software trigger or external pin trigger
- Analog Comparator
  - Up to 2 comparator analog modules
  - External input or internal band gap voltage selectable at negative node
  - Interrupt when compare result change
  - Power down wake up
- EBI (External Bus Interface) for external memory-mapped device access
  - Accessible space: 64KB in 8-bit mode or 128KB in 16-bit mode
  - Supports 8-bit/16-bit data width
  - Supports byte-write in 16-bit data width
- In-System Programming (ISP) and In-Circuit Programming (ICP)
- One built-in temperature sensor with 1°C resolution
- Brown-Out Detector
  - With 4 levels: 4.3V/3.7V/2.7V/2.2V
  - Supports Brown-Out interrupt and reset option
- 96-bit unique ID



- LVR (Low Voltage Reset)
  - Threshold voltage levels: 2.0V
- Operating Temperature: -40°C ~85°C
- Packages:
  - Green package (RoHS)
  - 48-pin LQFP, 33-pin QFN

## 3 BLOCK DIAGRAM

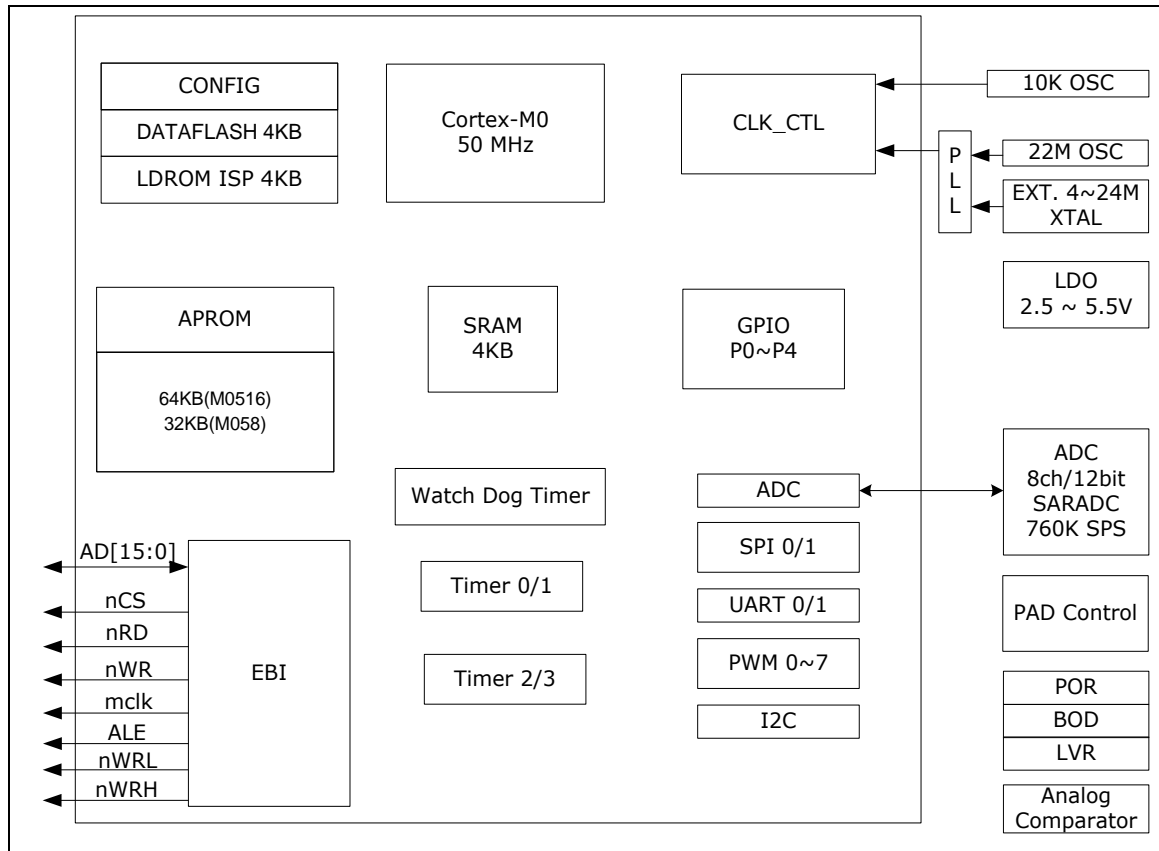


Figure 3-1 NuMicro™ M051 Series Block Diagram

## 4 SELECTION TABLE

NuMicro M051™ Series Selection Guide

Part number	APROM	RAM	Data Flash	LDROM	I/O	Timer	Connectivity			COMP	PWM	ADC	EBI	ISP ICP	Package
							UART	SPI	I2C						
M058LBN	32KB	4KB	4KB	4KB	40	4x32-bit	2	2	1	2	8	8X12-bit	v	v	LQFP48
M058ZBN	32KB	4KB	4KB	4KB	24	4x32-bit	2	1	1	2	5	8X12-bit		v	QFN33
M0516LBN	64KB	4KB	4KB	4KB	40	4x32-bit	2	2	1	2	8	8X12-bit	v	v	LQFP48
M0516ZBN	64KB	4KB	4KB	4KB	24	4x32-bit	2	1	1	2	5	8X12-bit		v	QFN33

Table 4-1 NuMicro™ M051 Series Product Selection Guide

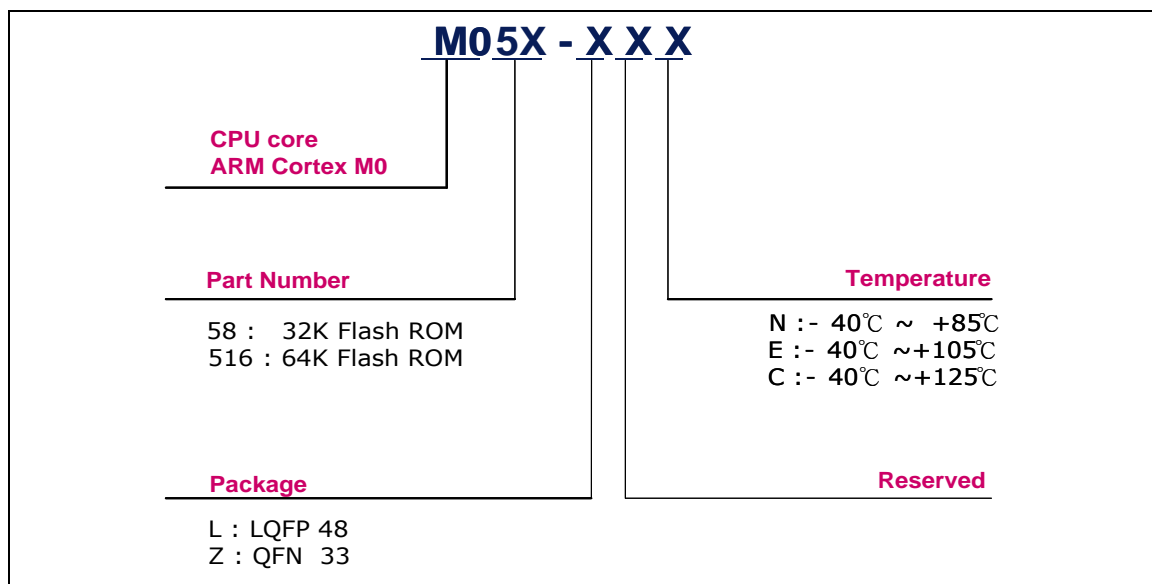


Figure 4-1 NuMicro™ Naming Rule

## 5 PIN CONFIGURATION

### 5.1 QFN 33 pin

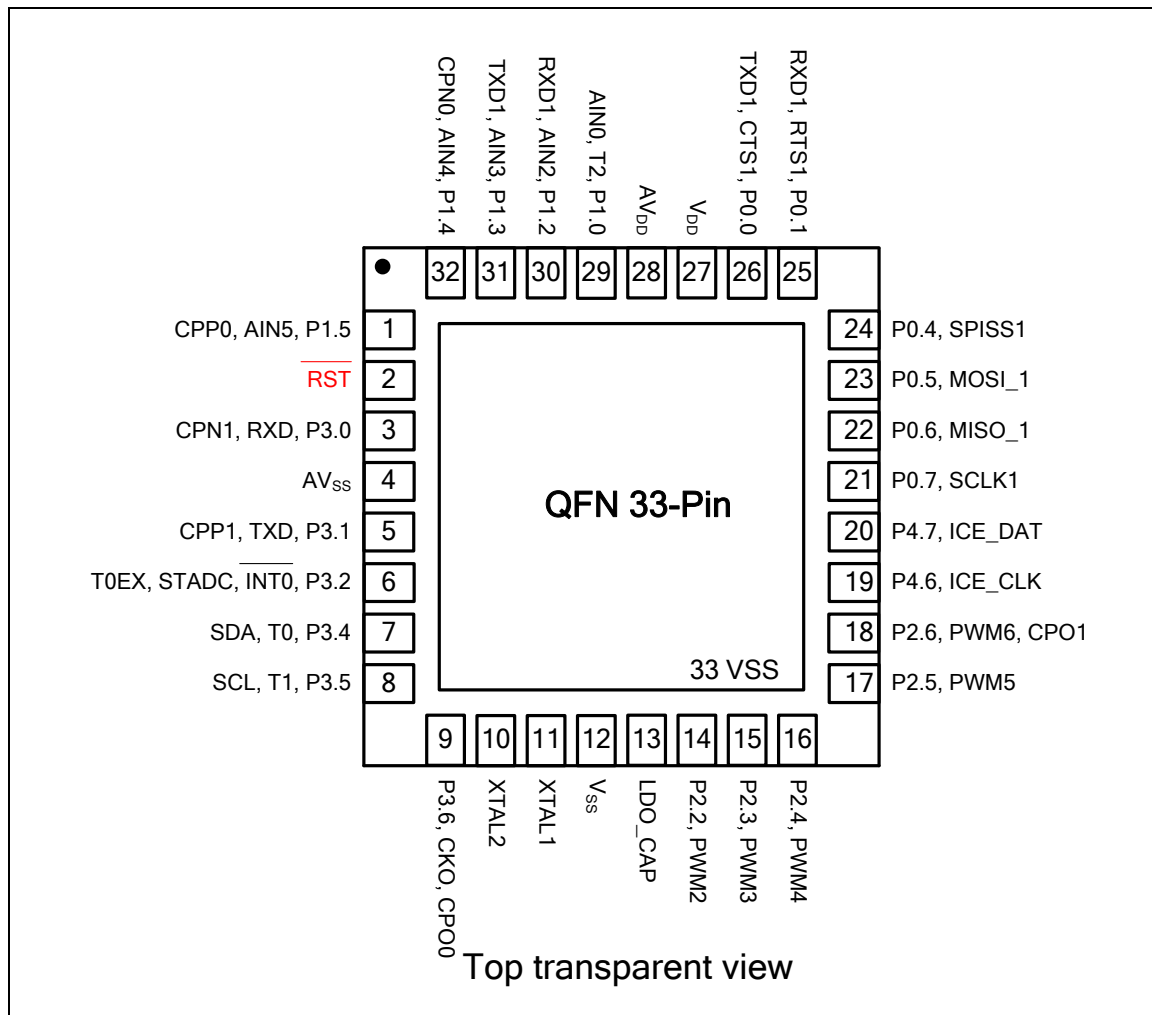


Figure 5-1 NuMicro™ M051 Series QFN33 Pin Diagram

## 5.2 LQFP 48 pin

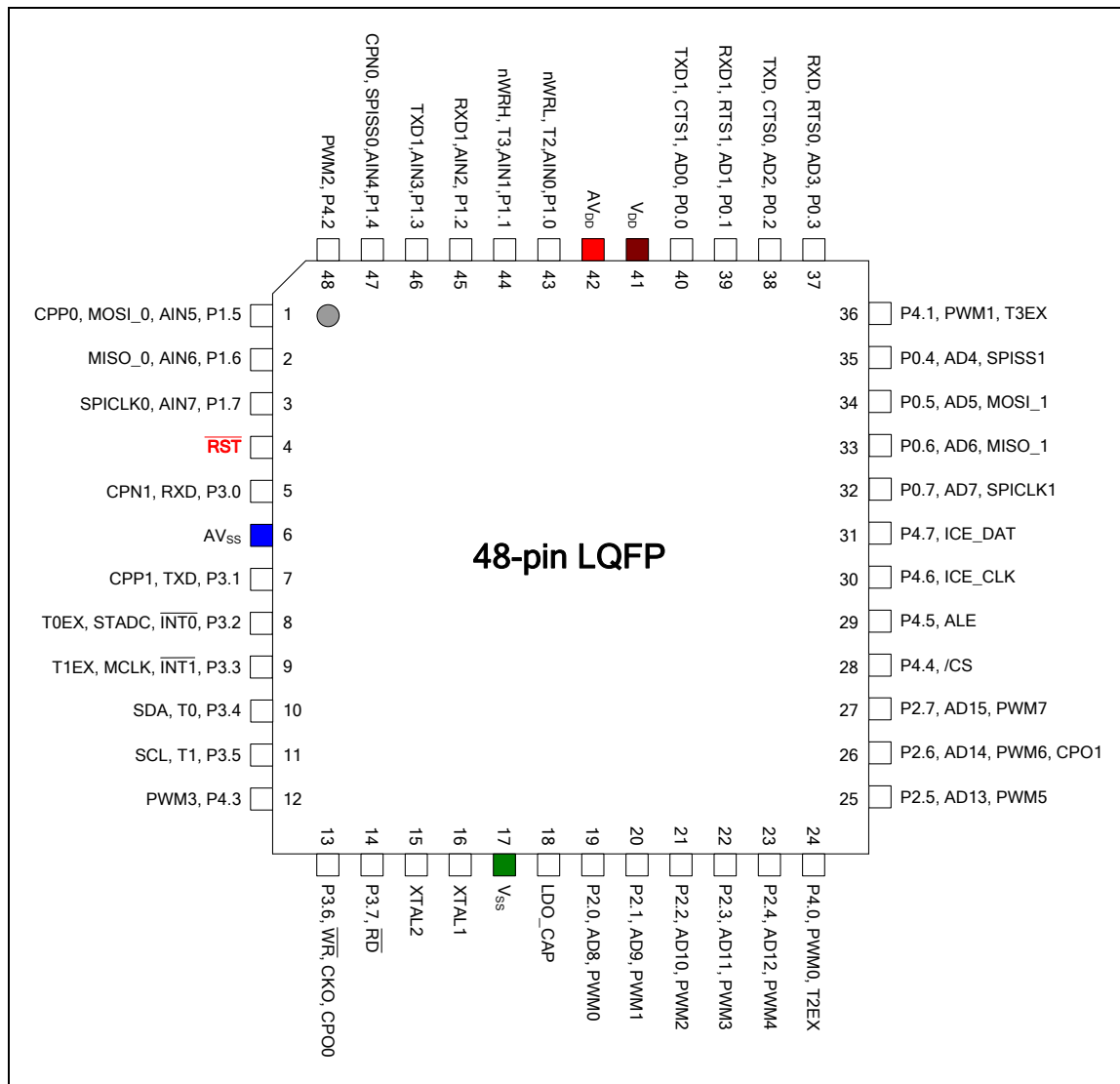
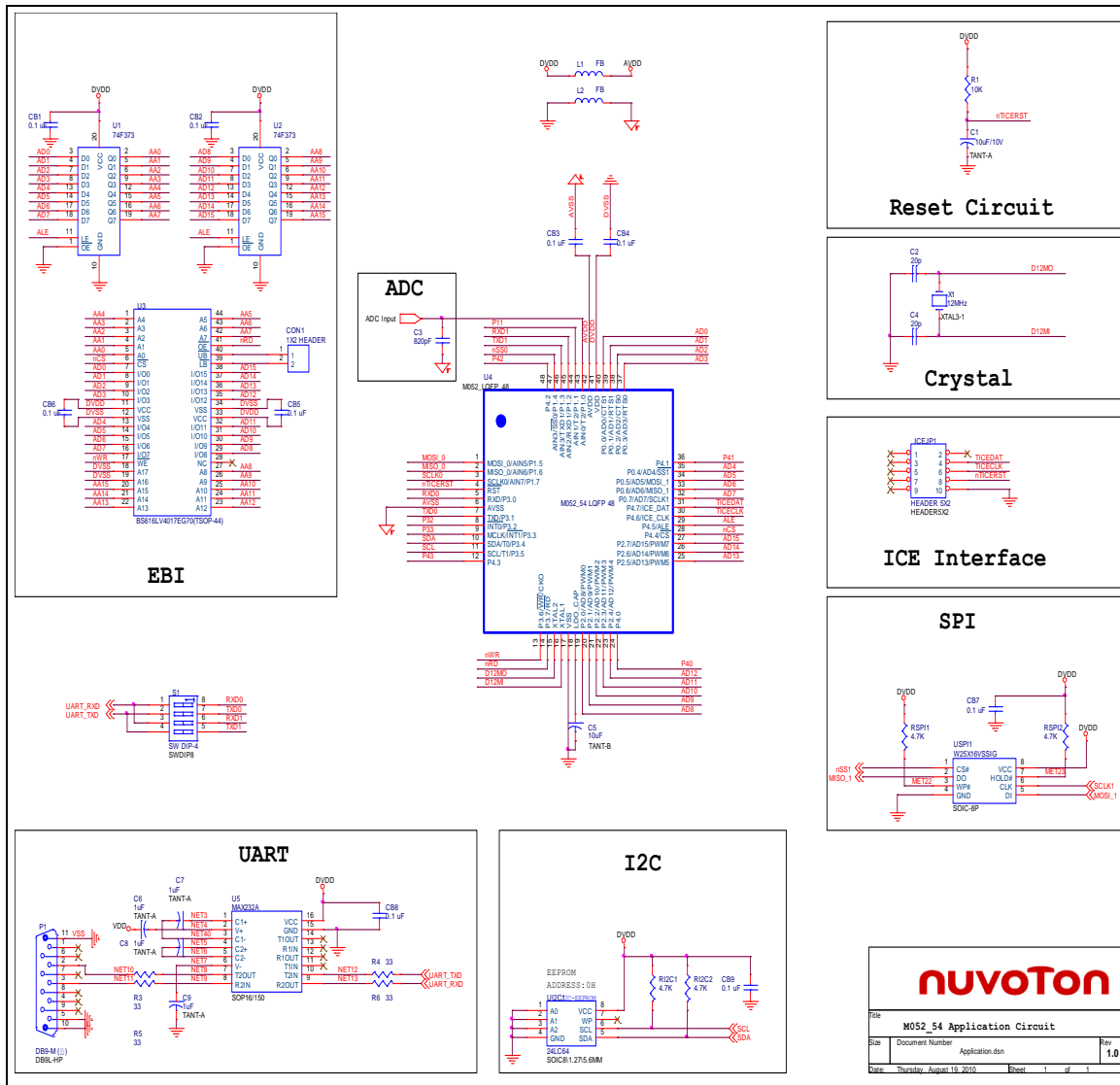


Figure 5-2 NuMicro™ M051 Series LQFP-48 Pin Diagram

### 6 TYPICAL APPLICATION CIRCUIT





## 7 ELECTRICAL CHARACTERISTICS

### 7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	$V_{DD} - V_{SS}$	-0.3	+7.0	V
Input Voltage	$V_{IN}$	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into $V_{DD}$		-	120	mA
Maximum Current out of $V_{SS}$			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

**Note:** Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.



## 7.2 DC Electrical Characteristics

( $V_{DD} - V_{SS} = 2.5 \sim 5.5V$ ,  $T_A = 25^\circ C$ ,  $F_{OSC} = 50\text{ MHz}$  unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	$V_{DD}$	2.5		5.5	V	$V_{DD} = 2.5V \sim 5.5V$ up to 50 MHz
LDO Output Voltage	$V_{LDO}$	1.7	1.8	1.9	V	$V_{DD} \geq 2.5V$
Band Gap Analog Input	$V_{BG}$	-5%	1.20	+5%	V	$V_{DD} = 2.5V \sim 5.5V$
Analog Operating Voltage	$AV_{DD}$	0		$V_{DD}$	V	
Analog Reference Voltage	$V_{ref}$	0		$AV_{DD}$	V	
Operating Current Normal Run Mode @ 50 MHz	IDD1		20.6		mA	$V_{DD} = 5.5V @ 50MHz$ , enable all IP and PLL, XTAL=12MHz
	IDD2		14.4		mA	$V_{DD} = 5.5V @ 50MHz$ , disable all IP and enable PLL, XTAL=12MHz
	IDD3		18.9		mA	$V_{DD} = 3.3V @ 50MHz$ , enable all IP and PLL, XTAL=12MHz
	IDD4		12.8		mA	$V_{DD} = 3.3V @ 50MHz$ , disable all IP and enable PLL, XTAL=12MHz
Operating Current Normal Run Mode @ 22Mhz	IDD5		6.2		mA	$V_{DD} = 5.5V @ 22MHz$ , enable all IP and IRC22M, disable PLL
	IDD6		3.4		mA	$V_{DD} = 5.5V @ 22MHz$ , disable all IP and enable IRC22M, disable PLL
	IDD7		6.1		mA	$V_{DD} = 3.3V @ 22MHz$ , enable all IP and IRC22M, disable PLL
	IDD8		3.4		mA	$V_{DD} = 3.3V @ 22MHz$ , disable all IP and enable IRC22M, disable PLL
Operating Current Normal Run Mode @ 12Mhz	IDD9		5.3		mA	$V_{DD} = 5.5V @ 12MHz$ , enable all IP and disable PLL, XTAL=12MHz
	IDD10		3.7		mA	$V_{DD} = 5.5V @ 12MHz$ , disable all IP and disable PLL, XTAL=12MHz
	IDD11		4.0		mA	$V_{DD} = 3.3V @ 12MHz$ , enable all IP and disable PLL, XTAL=12MHz
	IDD12		2.3		mA	$V_{DD} = 3.3V @ 12MHz$ , disable all IP and disable PLL, XTAL=12MHz



PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Current Normal Run Mode @ 4 MHz	IDD13		3.4		mA	V <sub>DD</sub> = 5.5V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	IDD14		2.6		mA	V <sub>DD</sub> = 5.5V@4MHz, disable all IP and disable PLL, XTAL=4MHz
	IDD15		2.0		mA	V <sub>DD</sub> = 3.3V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	IDD16		1.3		mA	V <sub>DD</sub> = 3.3V@4MHz, disable all IP and disable PLL, XTAL=4MHz
Operating Current Normal Run Mode @ 10Khz	IDD17		98.7		uA	V <sub>DD</sub> = 5.5V@10KHz, enable all IP and IRC10K, disable PLL
	IDD18		97.4		uA	V <sub>DD</sub> = 5.5V@10KHz, disable all IP and enable IRC10K, disable PLL
	IDD19		86.4		uA	V <sub>DD</sub> = 3.3V@10KHz, enable all IP and IRC10K, disable PLL
	IDD20		85.2		uA	V <sub>DD</sub> = 3.3V@10KHz, disable all IP and enable IRC10K, disable PLL
Operating Current Idle Mode @ 50 MHz	IIDLE1		16.2		mA	V <sub>DD</sub> = 5.5V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	IIDLE2		10.0		mA	V <sub>DD</sub> = 5.5V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
	IIDLE3		14.6		mA	V <sub>DD</sub> = 3V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	IIDLE4		8.5		mA	V <sub>DD</sub> = 3V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 22Mhz	IIDLE5		4.3		mA	V <sub>DD</sub> = 5.5V@22MHz, enable all IP and IRC22M, disable PLL
	IIDLE6		1.5		mA	V <sub>DD</sub> = 5.5V@22MHz, disable all IP and enable IRC22M, disable PLL
	IIDLE7		4.2		mA	V <sub>DD</sub> = 3.3V@22MHz, enable all IP and IRC22M, disable PLL
	IIDLE8		1.4		mA	V <sub>DD</sub> = 3.3V@22MHz, disable all IP and enable IRC22M, disable PLL
Operating Current Idle Mode	IIDLE9		4.3		mA	V <sub>DD</sub> = 5.5V@12MHz, enable all IP and disable PLL, XTAL=12MHz



PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
@ 12 MHz	IIDLE10		2.6		mA	V <sub>DD</sub> = 5.5V@12MHz, disable all IP and disable PLL, XTAL=12MHz
	IIDLE11		2.9		mA	V <sub>DD</sub> = 3.3V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	IIDLE12		1.3		mA	V <sub>DD</sub> = 3.3V@12MHz, disable all IP and disable PLL, XTAL=12MHz
Operating Current Idle Mode @ 4 MHz	IIDLE13		3.0		mA	V <sub>DD</sub> = 5.5V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	IIDLE14		2.3		mA	V <sub>DD</sub> = 5.5V@4MHz, disable all IP and disable PLL, XTAL=4MHz
	IIDLE15		1.7		mA	V <sub>DD</sub> = 3.3V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	IIDLE16		1.0		mA	V <sub>DD</sub> = 3.3V@4MHz, disable all IP and disable PLL, XTAL=4MHz
Operating Current Idle Mode @ 10Khz	IIDLE17		97.8		uA	V <sub>DD</sub> = 5.5V@10KHz, enable all IP and IRC10K, disable PLL
	IIDLE18		96.5		uA	V <sub>DD</sub> = 5.5V@10KHz, disable all IP and enable IRC10K, disable PLL
	IIDLE19		85.5		uA	V <sub>DD</sub> = 3.3V@10KHz, enable all IP and IRC10K, disable PLL
	IIDLE20		84.4		uA	V <sub>DD</sub> = 3.3V@10KHz, disable all IP and enable IRC10K, disable PLL
Standby Current Power-down Mode (Deep Sleep Mode)	IPWD1		10		μA	V <sub>DD</sub> = 5.5V, No load @ Disable BOV function
	IPWD2		10		μA	V <sub>DD</sub> = 3.0V, No load @ Disable BOV function
Input Current P0/1/2/3/4 (Quasi-bidirectional mode)	IIN1	-75	-	+15	μA	V <sub>DD</sub> = 5.5V, VIN = 0V or VIN= V <sub>DD</sub>
Input Leakage Current P0/1/2/3/4	ILK	-1	-	+1	μA	V <sub>DD</sub> = 5.5V, 0<VIN< V <sub>DD</sub>
Input Low Voltage P0/1/2/3/4 (TTL input)	VIL1	-0.3	-	0.8	V	V <sub>DD</sub> = 4.5V
		-0.3	-	0.6		V <sub>DD</sub> = 2.5V
Input High Voltage P0/1/2/3/4 (TTL input)	VIH1	2.0	-	V <sub>DD</sub> +0.2	V	V <sub>DD</sub> = 5.5V



PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
		1.5	-	$V_{DD} + 0.2$		$V_{DD} = 3.0V$
Input Low Voltage XT1[*2]	VIL3	0	-	0.8	V	$V_{DD} = 4.5V$
		0	-	0.4		$V_{DD} = 2.5V$
Input High Voltage XT1[*2]	VIH3	3.5	-	$V_{DD} + 0.2$	V	$V_{DD} = 5.5V$
		2.4	-	$V_{DD} + 0.2$		$V_{DD} = 3.0V$
Negative going threshold (Schmitt input), /RST	VILS	-0.5	-	$0.2 V_{DD}$	V	
Positive going threshold (Schmitt input), /RST	VIHS	$0.7 V_{DD}$	-	$V_{DD} + 0.5$	V	
Internal /RST pin pull up resistor	RRST	40		150	K $\Omega$	
Negative going threshold (Schmitt input), P0/1/2/3/4	VILS	-0.5	-	$0.3 V_{DD}$	V	
Positive going threshold (Schmitt input), P0/1/2/3/4	VIHS	$0.7 V_{DD}$	-	$V_{DD} + 0.5$	V	
Source Current P0/1/2/3/4 (Quasi- bidirectional Mode)	ISR11	-300	-370	-450	$\mu A$	$V_{DD} = 4.5V, V_S = 2.4V$
	ISR12	-50	-70	-90	$\mu A$	$V_{DD} = 2.7V, V_S = 2.2V$
	ISR13	-40	-60	-80	$\mu A$	$V_{DD} = 2.5V, V_S = 2.0V$
Source Current P0/1/2/3/4 (Push-pull Mode)	ISR21	-20	-24	-28	mA	$V_{DD} = 4.5V, V_S = 2.4V$
	ISR22	-4	-6	-8	mA	$V_{DD} = 2.7V, V_S = 2.2V$
	ISR23	-3	-5	-7	mA	$V_{DD} = 2.5V, V_S = 2.0V$
Sink Current P0/1/2/3/4 (Quasi-bidirectional and Push-pull Mode)	ISK11	10	16	20	mA	$V_{DD} = 4.5V, V_S = 0.45V$
	ISK12	7	10	13	mA	$V_{DD} = 2.7V, V_S = 0.45V$
	ISK13	6	9	12	mA	$V_{DD} = 2.5V, V_S = 0.45V$
Brown-Out voltage with BOV_VL [1:0] =00b	VBO2.2	2.0	2.2	2.4	V	$V_{DD} = 5.5V$
Brown-Out voltage with BOV_VL [1:0] =01b	VBO2.7	2.5	2.7	2.9	V	$V_{DD} = 5.5V$
Brown-Out voltage with BOV_VL [1:0] =10b	VBO3.8	3.5	3.7	3.9	V	$V_{DD} = 5.5V$
Brown-Out voltage with BOV_VL [1:0] =11b	VBO4.5	4.1	4.3	4.5	V	$V_{DD} = 5.5V$
Hysteresis range of BOD voltage	VBH	30	-	150	mV	$V_{DD} = 2.5V \sim 5.5V$

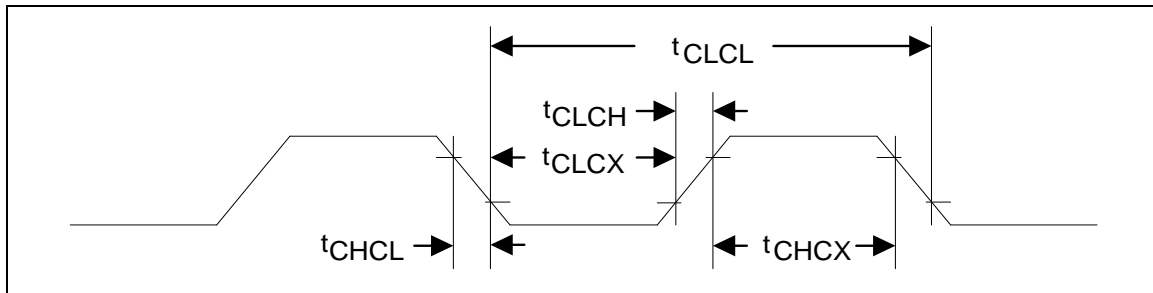
**Notes:**

1. /RST pin is a Schmitt trigger input.
2. XTAL1 is a CMOS input.
3. Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. In the condition of  $V_{DD}=5.5V$ , the transition current reaches its maximum value when  $V_{in}$  approximates to 2V.



## 7.3 AC Electrical Characteristics

### 7.3.1 External Crystal



**Note:** Duty cycle is 50%.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITION
Clock High Time	$t_{CHCX}$	20	-	-	nS	
Clock Low Time	$t_{CLCX}$	20	-	-	nS	
Clock Rise Time	$t_{CLCH}$	-	-	10	nS	
Clock Fall Time	$t_{CHCL}$	-	-	10	nS	

### 7.3.2 External Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	°C
$V_{DD}$	-	2.5	5	5.5	V
Operating current	12 MHz@ $V_{DD} = 5V$	-	1	-	mA

## 7.3.3 Typical Crystal Application Circuits

CRYSTAL	C1	C2
4 MHz ~ 24 MHz	Optional (Depend on crystal specification)	

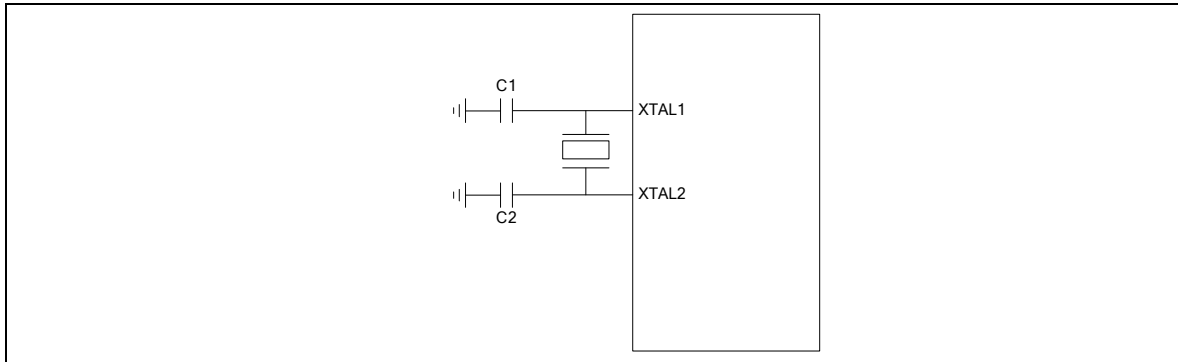


Figure 7-1 Typical Crystal Application Circuit



## 7.3.4 Internal 22.1184 MHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Center Frequency	-	-	22.1184		MHz
Calibrated Internal Oscillator Frequency	+25 °C; $V_{DD}=5V$	-3	-	+3	%
	-40 °C~+85 °C; $V_{DD}=2.5V\sim5.5V$	-5	-	+5	%
Operating current	$V_{DD}=5V$	-	500	-	uA

## 7.3.5 Internal 10kHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage <sup>[1]</sup>	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25 °C; $V_{DD}=5V$	-30	-	+30	%
	-40 °C~+85 °C; $V_{DD}=2.5V\sim5.5V$	-50	-	+50	%
Operating current	$V_{DD}=5V$	-	5	-	uA

**Notes:**

1. Internal operation voltage comes from LDO.



## 7.4 Analog Characteristics

### 7.4.1 Specification of 12-bit SARADC

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
Resolution	-	-	-	12	Bit
Differential nonlinearity error	DNL	-	±1.2	-	LSB
Integral nonlinearity error	INL	-	±1.2	-	LSB
Offset error	EO	-	+3	+5	LSB
Gain error (Transfer gain)	EG	-	-4	-6	-
Monotonic	-	Guaranteed			-
ADC clock frequency	FADC	-	-	16	MHz
Conversion time	TADC	-	13	-	Clock
Sample rate	FS	-	-	760	K SPS
Supply voltage	V <sub>LDO</sub>	-	1.8	-	V
	V <sub>ADD</sub>	3	-	5.5	V
Supply current (Avg.)	IDD	-	0.5	-	mA
	IDDA	-	1.5	-	mA
Input voltage range	V <sub>IN</sub>	0	-	AV <sub>DD</sub>	V
Capacitance	C <sub>IN</sub>	-	5	-	pF



## 7.4.2 Specification of LDO & Power management

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.5	5	5.5	V	$V_{DD}$ input voltage
Output Voltage	-10%	1.8	+10%	V	LDO output voltage
Temperature	-40	25	85	°C	
C	-	1u	-	F	Resr=1ohm

**Note:**

1. It is recommended a 100nF bypass capacitor is connected between  $V_{DD}$  and the closest  $V_{SS}$  pin of the device.
2. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest  $V_{SS}$  pin of the device.



## 7.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	5	5.5	V
Temperature	-	-40	25	85	°C
Quiescent current	V <sub>DD</sub> =5.5V	-	-	5	uA
Threshold voltage	Temperature=25°	1.7	2.0	2.3	V
	Temperature=-40°	-	2.3	-	V
	Temperature=85°	-	1.8	-	V
Hysteresis	-	0	0	0	V

## 7.4.4 Specification of Brown-Out Detector

Parameter	Condition	Min.	Typ.	Max.	Unit
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV <sub>DD</sub> =5.5V	-	-	140	μA
Temperature	-	-40	25	85	°C
Brown-Out voltage	BOV_VL[1:0]=11	4.1	4.3	4.5	V
	BOV_VL [1:0]=10	3.5	3.7	3.9	V
	BOV_VL [1:0]=01	2.5	2.7	2.9	V
	BOV_VL [1:0]=00	2.0	2.2	2.4	V
Hysteresis	-	30m	-	150m	V

## 7.4.5 Specification of Power-On Reset (5V)

Parameter	Condition	Min.	Typ.	Max.	Unit
Temperature	-	-40	25	85	°C
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA



## 7.4.6 Specification of Temperature Sensor

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage <sup>[1]</sup>		1.62	1.8	1.98	V
Temperature		-40	-	85	°C
Gain		-1.72	-1.76	-1.80	mV/°C
Offset	Temp=0 °C	717	725	733	mV

Note[1]: Internal operation voltage comes from LDO.

## 7.4.7 Specification of Comparator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	°C
V <sub>DD</sub>	-	2.4	3	5.5	V
V <sub>DD</sub> current	-	-	40	80	uA
Input offset voltage	-		10	20	mV
Output swing	-	0.1	-	V <sub>DD</sub> -0.1	V
Input common mode range	-	0.1	-	V <sub>DD</sub> -0.1	V
DC gain	-	-	70	-	dB
Propagation delay	@VCM=1.2 V and VDIFF=0.1 V	-	200	-	ns
Hysteresis	@VCM=0.2 V ~ V <sub>DD</sub> -0.2V	-	±10	-	mV
Stable time	@CINP=1.3 V CINN=1.2 V	-	-	2	us



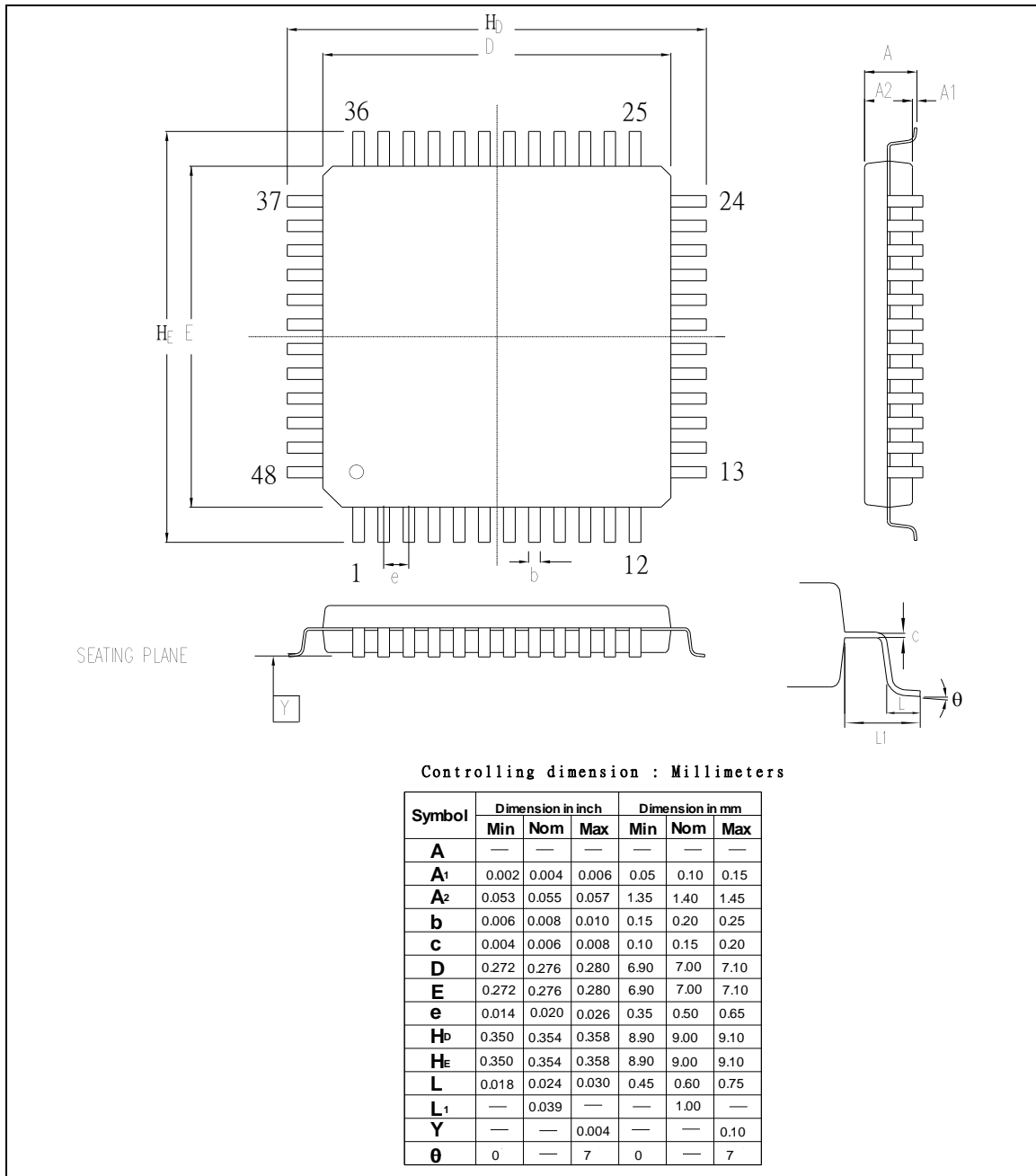
## 7.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
N <sub>endu</sub>	Endurance		100000			cycles <sup>[1]</sup>
T <sub>ret</sub>	Retention time	Temp=85 °C	10			year
T <sub>erase</sub>	Page erase time		19	20	21	ms
T <sub>mess</sub>	Mess erase time		30	40	50	ms
T <sub>prog</sub>	Program time		38	40	42	us
V <sub>DD</sub>	Supply voltage		1.62	1.8	1.98	V <sup>[2]</sup>
I <sub>dd1</sub>	Read current				0.25	mA
I <sub>dd2</sub>	Program/Erase current				7	mA
I <sub>pd</sub>	Power down current			1	20	uA

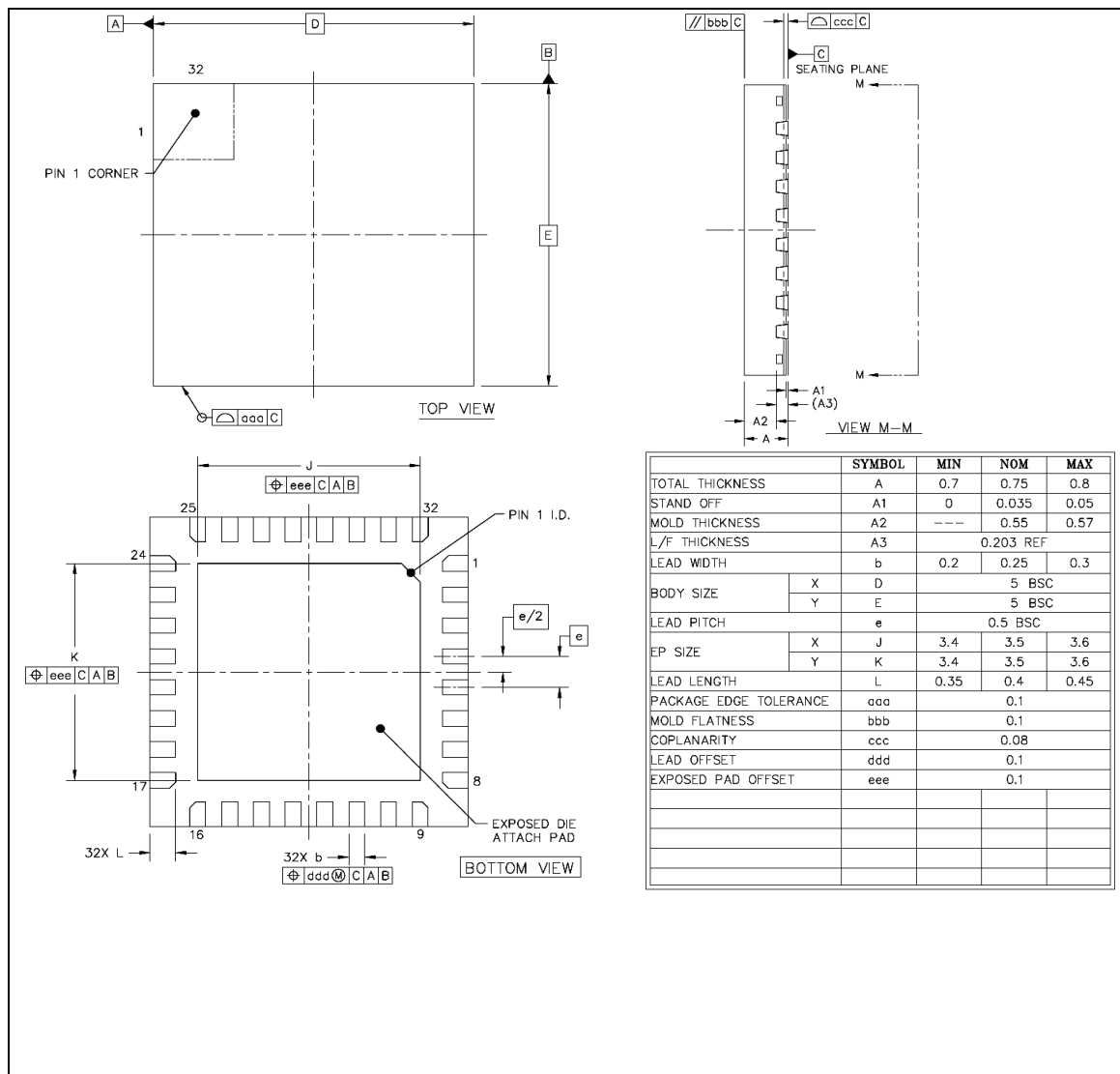
1. Number of program/erase cycles.
2. V<sub>DD</sub> is source from chip LDO output voltage.
3. Guaranteed by design, not test in production.

### 8 PACKAGE DIMENSIONS

#### 8.1 LQFP-48 (7x7x1.4mm<sup>2</sup> Footprint 2.0mm)



## 8.2 QFN-33 (5X5 mm<sup>2</sup>, Thickness 0.8mm, Pitch 0.5 mm)





## 9 REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
V1.0	Oct 20, 2011	-	Initial issued
V1.01	Mar. 19, 2012	7.3.4	Updated the Center Frequency of 22Mhz RC spec



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