ARM Cortex™-M0

32-BIT MICROCONTROLLER

NuMicro™ Family
Mini51 系列产品简介

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 概述

NuMicro MINI51™ 系列是32位的微处理器，内嵌ARM® Cortex™-M0内核，可用于工业控制和需要高性能、低功耗的应用. Cortex™-M0是ARM最新的微处理器，有32位的性能，但是价格只相当于传统的8位单片机.

NuMicro MINI51™系列最快可以跑到24MHz. 因而可以支持很广范围的工业控制和需要高性能CPU的场合. NuMicro MINI51™ 系列内嵌4K/8K/16K字节程序flash，数据flash大小可配置(与程序flash共享) ,2K字节ISP flash，2K字节SRAM.

为了降低成本，减小空间，NuMicro MINI51™ 系列内嵌了很多外设，像：I/O口、定时器、UART、SPI、I2C、PWM、ADC、看门狗和低电压检测，这使NuMicro MINI51™ 系列可以用于更广泛的应用.

另外，NuMicro MINI51™ 系列还配备ISP (In-System Programming) 和 ICP (In-Circuit Programming) 功能，让用户可以升级固件而不必将芯片从板子上取下.

2 特性

- 内核
  - ARM® Cortex™-M0 核，最高跑到 24 MHz
  - 一个 24比特系统定时器
  - 支持低功耗Idle 模式
  - 一个单指令周期硬件乘法器
  - 支持32个外部中断的NVIC, 每个中断有4级优先级
  - 支持串行调试接口 (SWD)，有2个监视点(watchpoints)/4个断点(breakpoints)
- 内嵌LDO 可支持宽电压输入: 2.5 V to 5.5 V
- 内存
  - 4KB/8KB/16KB Flash 内存用来存放应用程序 (APROM)
  - 可配置的数据 flash(Data Flash)
  - 2KB启动代码空间 (LDROM)
  - 内嵌2KB SRAM (SRAM)
- 支持In-System Programming (ISP) & In-Circuit Programming (ICP)
- 时钟控制
  - 系统时钟源可编程
    - 正在运行代码时可以切换时钟源
  - 4 ~ 24 MHz crystal oscillator (HXT)
  - 32.768K crystal oscillator (LXT)，可用于系统时钟和在掉电模式(power down mode)下唤醒CPU (如果外设选择32.768K作为时钟源的话)
  - 22.1184 MHz 内部 oscillator (HIRC) (25^{0}C, 5V,1% 误差)
    - 在-40^{0}C to 85^{0}C，利用外部32.768K晶振可以动态矫正到22 MHz +/- 1%
  - 10 KHz 内部低功耗oscillator (LIRC)，给看门狗和掉电模式下唤醒CPU提供时钟源(如果外设选择10K作为时钟源的话)
- I/O口
  - LQFP-48封装，最多 30个通用 (GPIO) 脚
  - 软件可以配置I/O口为以下模式
    - 准双向输入/输出模式
    - 推挽输出
    - 开漏输出
    - 输入模式，带内部高阻

- 可选择施密特触发输入模式

- 定时器
  - 两个24-bit 定时器，有8-bit预分频
    - 支持 事件计数功能
    - 支持toggle输出模式
    - 脉冲宽度测量模式下，支持外部触发
      - 脉冲宽度捕获模式下，支持外部触发
- 看门狗定时器
  - 时钟源和超时周期可选择
  - 掉电和idle模式下支持唤醒CPU功能
  - 当超时发生时，可以选择发生中断还是复位CPU
- PWM
  - 内嵌最多3个16位PWM发生器，提供6个独立的PWM输出或者3组互补的PWM输出
  - 支持边沿对齐和中心对齐
  - 支持故障侦测
  - 每个PWM发生器有单独的时钟源，时钟除频，8比特预分频和死区发生器
  - 每个PWM周期可以发生中断
- UART
  - 一组 UART
  - 两个16字节的接收和发送缓冲区
  - 流控功能(CTSn 和 RTSn)
  - 支持 IrDA (SIR) 功能
  - 波特率可编程，最快可达 1/16 系统时钟
  - 支持 RS-485 功能
- SPI
  - 一组SPI
  - 主模式最高可达12 MHz, 从模式最高可达4 MHz
  - 支持SPI主/从模式
  - 全双工同步串行数据传输
  - 每笔传输比特长度可配置，范围 1到 32 比特
  - MSB 或者 LSB优先
  - 发送和 接收边沿独立，都可以上升沿也可以下降沿

- 32比特长度下，支持字节suspend 功能

- I^2C
  - 支持主/从模式
  - 主和从之间双向数据传输
  - 支持多主总线 (无核心主设备)
  - 同时发起传输的主设备之间仲裁，防止数据被破坏
  - 串行时钟同步，允许同一个总线上的设备有不同的比特率
  - 串行时钟同步可以用做一个握手机制，挂起或者重启串行传输
  - 时钟源可编程以方便波特率控制
  - 支持多地址识别(四个从地址，有掩码功能)
- ADC
  - 10-bit SAR型 ADC，速率 150K SPS
  - 最多8个single-end输入通道，一个内部band-gap输入
  - 可由软件或者外部引脚触发一次转换
- Analog Comparator
  - 2组模拟比较器。支持可编程的16级内部参考电压
  - 内嵌比较器参考电压(CRV)
- BOD R复位
  - 3种检测电压选择: 3.8V/2.7V/2.0V (缺省 2.0V)
  - BOD中断还是复位可选择
- 96比特唯一序列号 (Unique ID)
- 工作温度:-40℃~85℃
- 封装:
  - Green package (RoHS)
  - LQFP 48-pin (7x7), QFN 33-pin (5x5), QFN 33-pin (4x4)

3 产品型号和引脚配置

3.1 NuMicro Mini51™系列选型表

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity			Comp.	PWM	ADC	ISP ICP	IRC 22.1184 MHz	Package
							UART	SPI	I^2C						
MINI51LAN	4 KB	2 KB	Configurable	2 KB	up to 30	2x32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI51ZAN	4 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(5x5)
MINI51TAN	4 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(4x4)
MINI52LAN	8 KB	2 KB	Configurable	2 KB	up to 30	2x32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI52ZAN	8 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(5x5)
MINI52TAN	8 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(4x4)
MINI54LAN	16 KB	2 KB	Configurable	2 KB	up to 30	2x32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI54ZAN	16 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(5x5)
MINI54TAN	16 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(4x4)

表 3.1-1 NuMicro Mini51™系列产品选型表

3.2 引脚配置

3.2.1 LQFP 48-pin

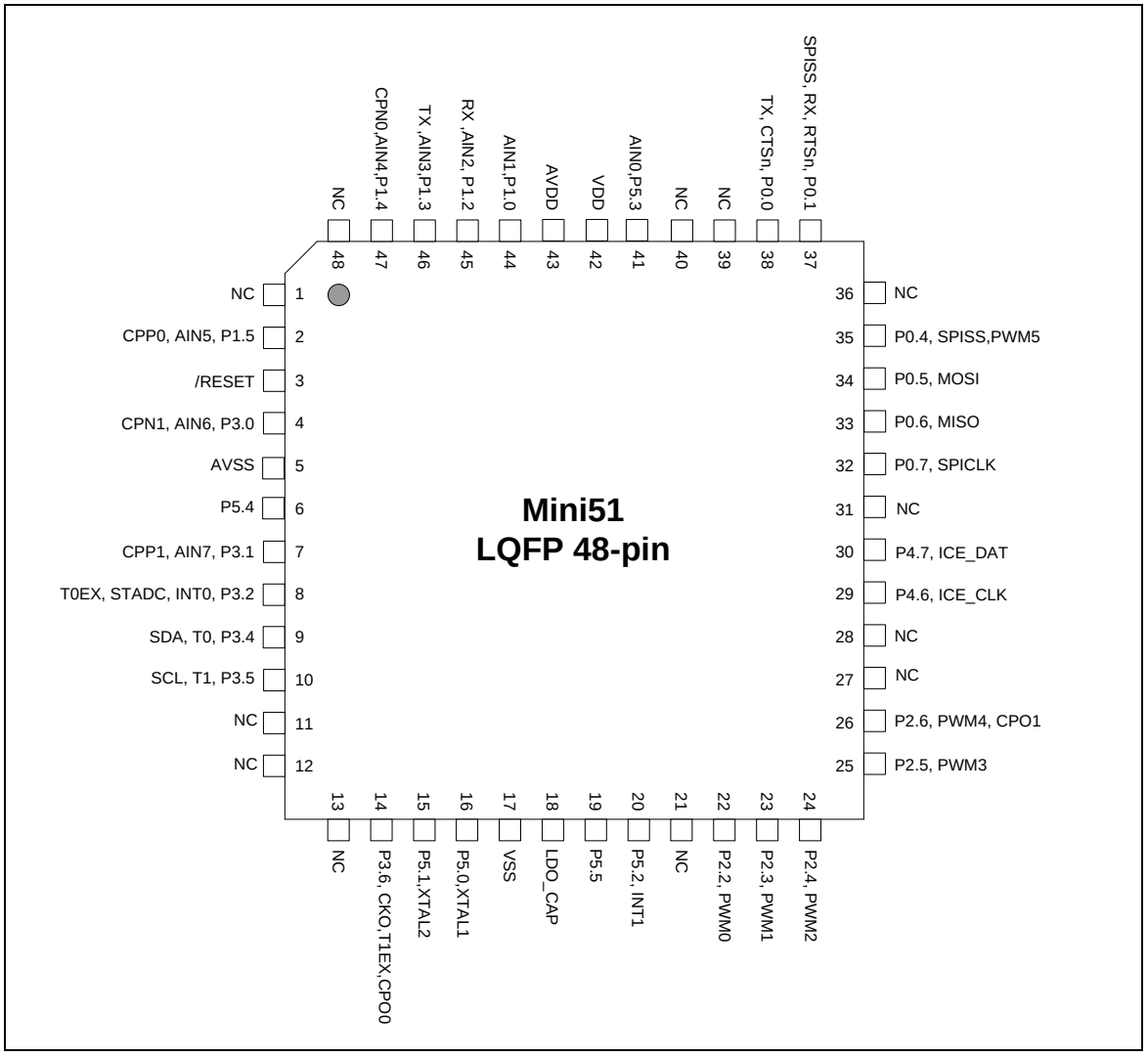


图 3.2-1 NuMicro Mini51™系列 LQFP 48-pin 图

3.2.2 QFN 33-pin

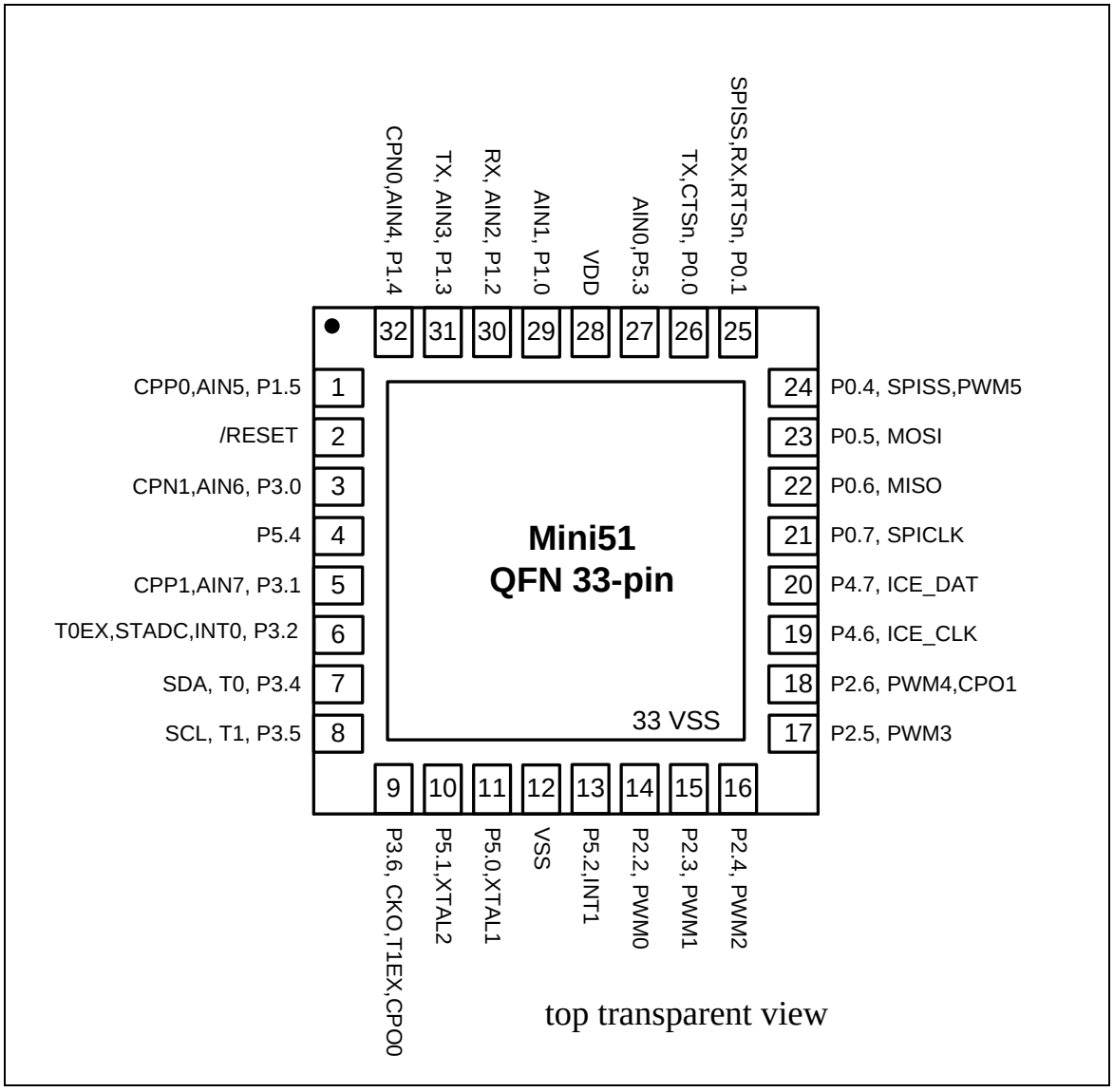


图 3.2-2 NuMicro Mini51™ 系列 QFN 33-pin 图

4 方块图

4.1 NuMicro Mini51™ 方块图

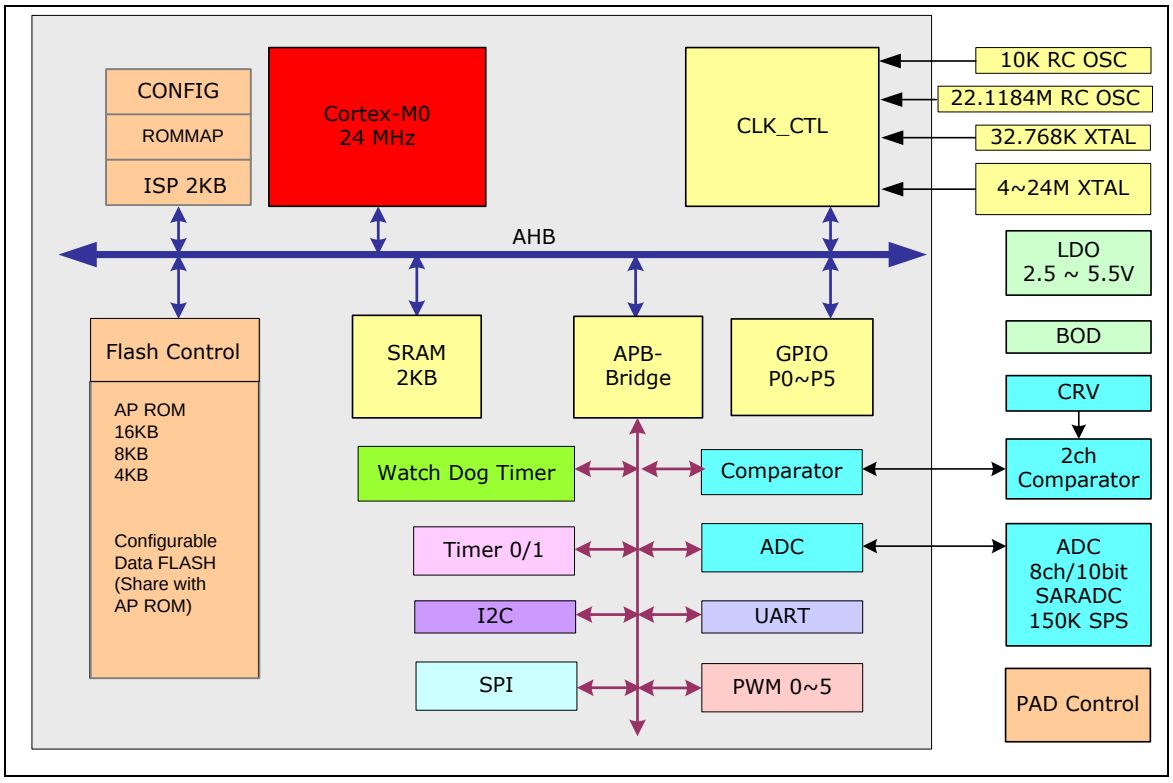
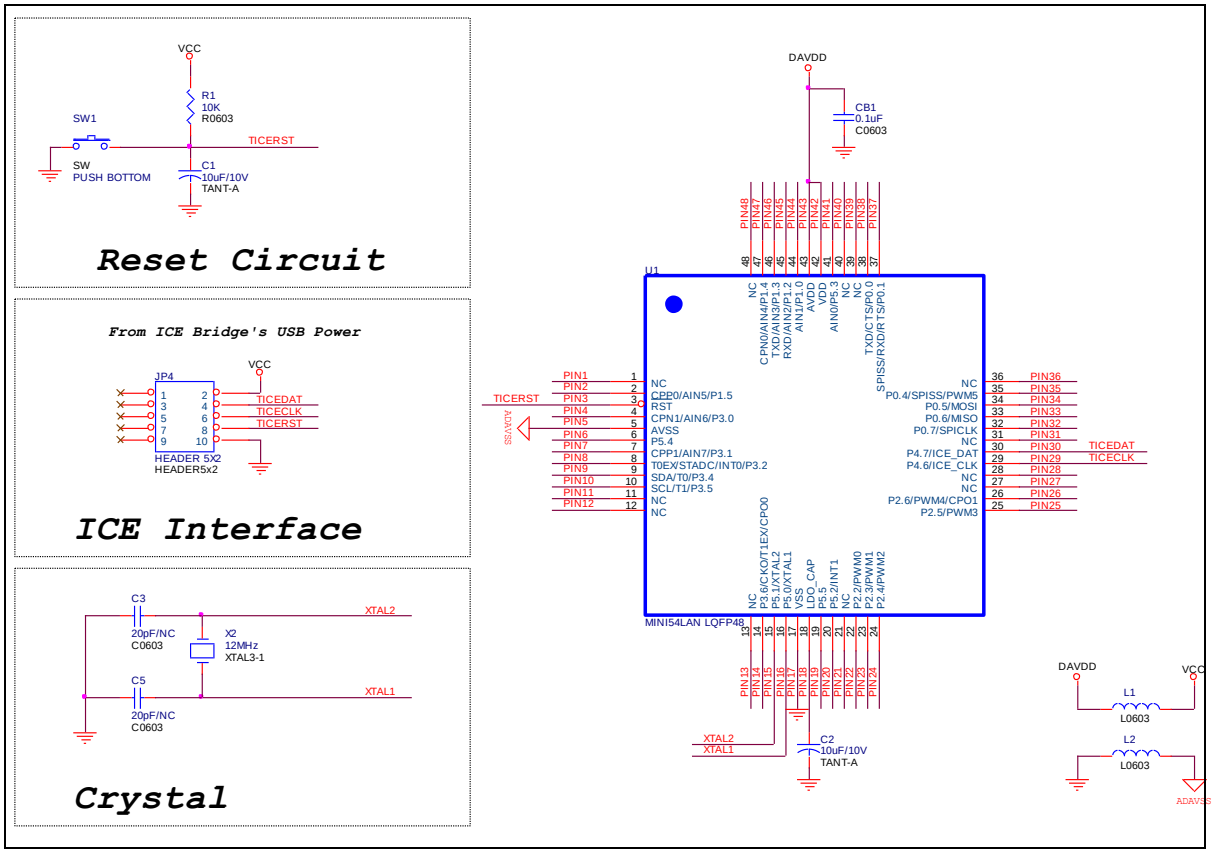


图 4.1-1 NuMicro Mini51™系列方块图

5 应用电路


VCC
R1
10K
R0603
SW1
TICERST
SW
PUSH BOTTOM
C1
10uF/10V
TANT-A
Reset Circuit
From ICE Bridge's USB Power
JP4
VCC
TICEDAT
TICECLK
TICERST
HEADER 5X2
HEADER5x2
ICE Interface
C3
20pF/NC
C0603
X2
12MHz
XTAL3-1
XTAL2
C5
20pF/NC
C0603
XTAL1
Crystal
DAVDD
CB1
0.1uF
C0603
U1
MINI54LAN LQFP48
TICERST
C2
10uF/10V
TANT-A
XTAL2
XTAL1
L1
L0603
L2
L0603
VCC
DAVDD

6 电器特性

6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into VDD		-	120	mA
Maximum Current out of VSS			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

6.2 DC 电器特性

(VDD-VSS=5.0 V, TA = 25°C, FOSC = 24 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5 V ~ 5.5 V up to 24 MHz
V_{DD} rise rate to ensure internal operation correctly	V_{RISE}	0.05			V/mS	
Power Ground	V_{SS} AV_{SS}	-0.3			V	
LDO Output Voltage	V_{LDO}	-10%	1.8	+10%	V	V_{DD} = 2.5V ~ 5.5V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Operating Current Normal Run Mode @ 24 MHz	I_{DD1}		9.5		mA	V_{DD} = 5.5V@24 MHz, enable all IP
	I_{DD2}		7.5		mA	V_{DD} = 5.5V@24 MHz, disable all IP
	I_{DD3}		7.5		mA	V_{DD} = 3.3V@24 MHz, enable all IP
	I_{DD4}		6		mA	V_{DD} = 3.3V@24 MHz, disable all IP
Operating Current Normal Run Mode @ 12 MHz	I_{DD5}		5.5		mA	V_{DD} = 5.5V@12 MHz, enable all IP
	I_{DD6}		4.5		mA	V_{DD} = 5.5V@12 MHz, disable all IP
	I_{DD7}		4		mA	V_{DD} = 3.3V@12 MHz, enable all IP
	I_{DD8}		3		mA	V_{DD} = 3.3V@12 MHz, disable all IP
Operating Current Normal Run Mode @ 4 MHz	I_{DD9}		3.6		mA	V_{DD} = 5.5V@4 MHz, enable all IP
	I_{DD10}		3.3		mA	V_{DD} = 5.5V@4 MHz, disable all IP
	I_{DD11}		1.7		mA	V_{DD} = 3.3V@4 MHz, enable all IP
	I_{DD12}		1.4		mA	V_{DD} = 3.3V@4 MHz, disable all IP
Operating Current Normal Run Mode @ 22.1184 MHz IRC	I_{DD13}		6.6		mA	V_{DD} = 5.5V@22.1184 MHz, enable all IP
	I_{DD14}		5		mA	V_{DD} = 5.5V@22.1184 MHz, disable all IP
	I_{DD15}		6.6		mA	V_{DD} = 3.3V@22.1184 MHz, enable all IP

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{DD16}		5		mA	V_{DD} = 3.3V@22.1184 MHz, disable all IP
Operating Current Normal Run Mode @ 32.768 KHz crystal oscillator	I_{DD17}		116		μA	V_{DD} = 5.5V@32.768 KHz, enable all IP
	I_{DD18}		113		μA	V_{DD} = 5.5V@32.768 KHz, disable all IP
	I_{DD19}		112		μA	V_{DD} = 3.3V@32.768 KHz, enable all IP
	I_{DD20}		100		μA	V_{DD} = 3.3V@32.768 KHz, disable all IP
Operating Current Normal Run Mode @ 10 KHz IRC	I_{DD21}		109		μA	V_{DD} = 5.5V@10 KHz, enable all IP
	I_{DD22}		108		μA	V_{DD} = 5.5V@10 KHz, disable all IP
	I_{DD23}		100		μA	V_{DD} = 3.3V@10 KHz, enable all IP
	I_{DD24}		98		μA	V_{DD} = 3.3V@10 KHz, disable all IP
Operating Current Idle Mode @ 24 MHz	I_{IDLE1}		5.5		mA	V_{DD} = 5.5V@24 MHz, enable all IP
	I_{IDLE2}		3.5		mA	V_{DD} = 5.5V@24 MHz, disable all IP
	I_{IDLE3}		3.8		mA	V_{DD} = 3.3V@24 MHz, enable all IP
	I_{IDLE4}		1.8		mA	V_{DD} = 3.3V@24 MHz, disable all IP
Operating Current Idle Mode @ 12 MHz	I_{IDLE5}		3.3		mA	V_{DD} = 5.5V@12 MHz, enable all IP
	I_{IDLE6}		2.6		mA	V_{DD} = 5.5V@12 MHz, disable all IP
	I_{IDLE7}		2		mA	V_{DD} = 3.3V@12 MHz, enable all IP
	I_{IDLE8}		1		mA	V_{DD} = 3.3V@12 MHz, disable all IP
Operating Current Idle Mode @ 4 MHz	I_{IDLE9}		3		mA	V_{DD} = 5.5V@4 MHz, enable all IP
	I_{IDLE10}		2.3		mA	V_{DD} = 5.5V@4 MHz, disable all IP
	I_{IDLE11}		1		mA	V_{DD} = 3.3V@4 MHz, enable all IP
	I_{IDLE12}		0.7		mA	V_{DD} = 3.3V@4 MHz, disable all IP
Operating Current Idle Mode	I_{IDLE13}		3.0		mA	V_{DD} = 5.5V@22.1184 MHz, enable all IP

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
@ 22.1184 MHz IRC	I_{IDLE14}		1.2		mA	V_{DD} = 5.5V@22.1184 MHz, disable all IP
	I_{IDLE15}		3.0		mA	V_{DD} = 3.3V@22.1184 MHz, enable all IP
	I_{IDLE16}		1.2		mA	V_{DD} = 3.3V@22.1184 MHz, disable all IP
Operating Current Idle Mode @ 32.768 KHz crystal oscillator	I_{IDLE17}		110		μA	V_{DD} = 5.5V@32.768 KHz, enable all IP
	I_{IDLE18}		107		μA	V_{DD} = 5.5V@32.768 KHz, disable all IP
	I_{IDLE19}		105		μA	V_{DD} = 3.3V@32.768 KHz, enable all IP
	I_{IDLE20}		102		μA	V_{DD} = 3.3V@32.768 KHz, disable all IP
Operating Current Idle Mode @ 10 KHz IRC	I_{IDLE21}		103		μA	V_{DD} = 5.5V@10 KHz, enable all IP
	I_{IDLE22}		102		μA	V_{DD} = 5.5V@10 KHz, disable all IP
	I_{IDLE23}		96		μA	V_{DD} = 3.3V@10 KHz, enable all IP
	I_{IDLE24}		95		μA	V_{DD} = 3.3V@10 KHz, disable all IP
Standby Current Power Down Mode	I_{PWD1}		10		μA	V_{DD} = 5.0V, CPU STOP All IP and Clock OFF
	I_{PWD2}		5		μA	V_{DD} = 3.3V, CPU STOP All IP and Clock OFF
Standby Current Power Down Mode with 32.768 KHz crystal enable	I_{PWD3}		12		μA	V_{DD} = 5.0V, CPU STOP All IP and Clock OFF except 32.768KHz crystal oscillator
	I_{PWD4}		7		μA	VDD = 3.3V, CPU STOP All IP and Clock OFF except 32.768KHz crystal oscillator
Input Current P0~P5 (Quasi-bidirectional mode)	I_{IN1}		-50	-60	μA	V_{DD} = 5.5 V, V_{IN} = 0 V or V_{IN}=V_{DD}
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3 V, V_{IN} = 0.45 V
Input Leakage Current PA, PB, PC, PD, PE	I_{LK}	-0.1	-	+0.1	μA	V_{DD} = 5.5 V, 0<V_{IN}<V_{DD}

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Logic 1 to 0 Transition Current PA~PE (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5 V, V_{IN}<2.0 V
Input Low Voltage P0~P5 (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
Input High Voltage P0~P5 (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} +0.2		V_{DD} = 3.0 V
Input Low Voltage P0~P5, (Schmitt input)	V_{IL2}		0.4 V_{DD}		V	
Input High Voltage P0~P5, (Schmitt input)	V_{IH2}		0.6 V_{DD}		V	
Hysteresis voltage of P0~P5 (Schmitt input)	V_{HY}		0.2 V_{DD}		V	
Input Low Voltage XT1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5 V
		0	-	0.4		V_{DD} = 3.0 V
Input High Voltage XT1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5 V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0 V
Internal /RESET pin pull up resistor	R_{RST}	40	-	100	KΩ	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	0.3 V_{DD}	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	0.6 V_{DD}	-	V_{DD}+0.5	V	
Source Current P0~P5. (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5 V, V_S = 2.0 V
Source Current P0~P5, (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5 V, V_S = 2.0 V
Sink Current P0~P5, (Quasi-	I_{SK1}	10	16	20	mA	V_{DD} = 4.5 V, V_S = 0.45 V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
bidirectional and Push-pull Mode)	I_{SK1}	7	10	13	mA	V_{DD} = 2.7 V, V_S = 0.45 V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5 V, V_S = 0.45 V

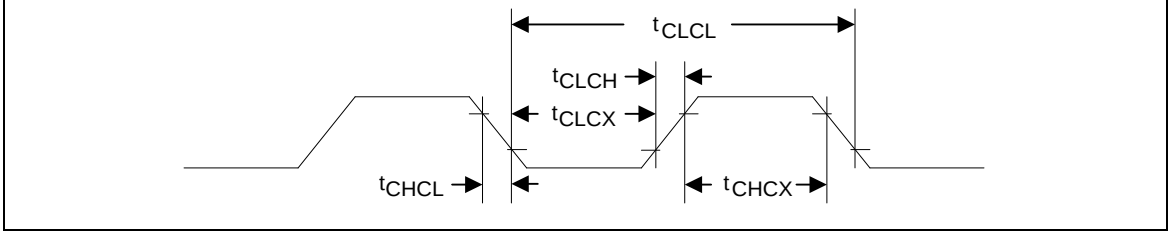
Note:

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of P0~P5 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, the transition current reaches its maximum value when V_{IN} approximates to 2 V.

6.3 AC 电器特性

6.3.1 External Input Clock

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
PARAMETER	tCHCX	20			nS	
Clock High Time	tCLCX	20			nS	
Clock Low Time	tCLCH			10	nS	
Clock Rise Time	tCHCL			10	nS	



Note: Duty cycle is 50%.

6.3.2 External 4~24 MHz XTAL Oscillator

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{HXTAL}	4	12	24	MHz	VDD = 2.5V ~ 5.5V
Temperature	T_{HXTAL}	-40		+85	°C	
Operating current	I_{HXTAL}		TBD		mA	VDD = 5.0V

6.3.3 Typical Crystal Application Circuits

CRYSTAL	C1	C2
4 MHz ~ 24 MHz	Optional (Depend on crystal specification)	

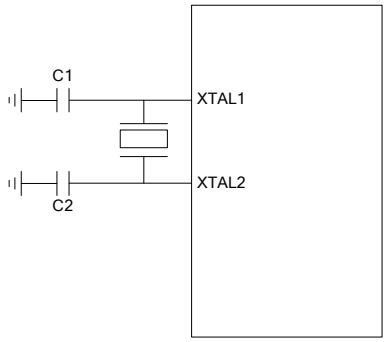


图 6.3-1 Typical Crystal Application Circuit

6.3.4 External 32.768 KHz XTAL Oscillator

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	fL_{XTAL}		32.768		KHz	VDD = 2.5V ~ 5.5V
Temperature	TL_{XTAL}	-40		+85	^{o}C	
Operating current	I_{HXTAL}		TBD		μA	VDD = 5.0V

6.3.5 Internal 22.1184 MHz RC Oscillator

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Supply voltage[1]	V_{HRC}		1.8		V	
Center Frequency	F_{HRC}	21.89	22.1184	22.34	MHz	25^{o}C, VDD = 5V
		20.57	22.1184	23.23	MHz	-40^{o}C~+85 ^{o}C, VDD = 2.5V~5.5V
		21.78	22.0	22.22	MHz	-40^{o}C~+85 ^{o}C, VDD = 2.5V~5.5V Enable 32.768K crystal oscillator and set TRIM_SEL = 1
Operating current	I_{HRC}		TBD		mA	

Note: Internal operation voltage comes from LDO

6.3.6 Internal 10 KHz RC Oscillator

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Supply voltage[1]	V_{LRC}		1.8		V	
Center Frequency	F_{LRC}	7	10	13	KHz	25°C, VDD = 5V
		5	10	15	KHz	-40°C~+85 °C, VDD = 2.5V~5.5V
Operating current	I_{LRC}		TBD		μA	VDD = 5V

Note: Internal operation voltage comes from LDO

.

6.4 模拟特性

6.4.1 Specification of Brown-Out Reset (BOD)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V_{BOD}	2.0		5.5	V	
Operating current	I_{BOD}		5	15	μA	VDD = 5V Enable BOD27 and BOD38
BOD38 detection level	V_{B38dt}	3.6	3.8	4.0	V	25°C
BOD27 detection level	V_{B27dt}	2.6	2.7	2.8	V	25°C

6.4.2 Specification of Low Voltage Reset (LVR)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V_{BOD}	2.0		5.5	V	
Operating current	I_{BOD}		1	2	μA	
Detection level	V_{LVR}		2.0		V	25°C
LVR always enable		1.6	2.0	2.4	V	-40°C ~ +85°C

6.4.3 Specification of Analog Comparator

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V_{BOD}	2.5	3.3	5.5	V	
Operating current	I_{CMP}		40	80	μA	
Input offset voltage	V_{OFFSET}		10	20	mV	
Output swing voltage	V_{swin}	0.1		V_{DD}-0.1	V	
Input common mode range (VCM)	V_{CM}	0.1		V_{DD}-0.1	V	
DC gain	G_{DC}		70		dB	
Propagation delay	T_{PDLY}		200		ns	VCM = 1.2V The difference voltage in CPPx and CPNx is 0.1V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Hysteresis	V_{HYS}		±10		mV	One bit control W/O & W. hysteresis @V_{CM}=0.2V ~ VDD-0.1V
Stable time	T_{STBL}			2	μS	CPPx = 1.3V and CPNX = 1.2V

6.4.4 Analog Comparator Reference Voltage (CRV)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V_{BOD}	2.5		5.5	V	
CRV step size	V_{STEP}		V_{DD}/24		V	VDD = 5V Enable BOD27 and BOD38
CRV output voltage absolute accuracy	A_{CRV}	-5		+5	%	
Unit resistor value	R_{CRV}		2K		ohm	

6.4.5 Specification of 10-bit ADC

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	AV_{DD}	2.7		5.5	V	AV_{DD} = V_{DD}
Operating current	I_{ADC}			1	mA	AV_{DD} = V_{DD} = 5V, F_{SPS} = 150K
Resolution	R_{ADC}			10	Bit	
Reference voltage	V_{REF}		A_{VDD}		V	V_{REF} connect to A_{VDD} in chip
ADC input voltage	V_{IN}	0		V_{REF}	V	
Conversion time	T_{CONV}	6.7			μS	
Sampling Rate	F_{SPS}	150K			Hz	V_{DD} = 5V, ADC clock = 6MHz Free running conversion
Integral Non-Linearity Error (INL)	INL			±1	LSB	
Differential Non-Linearity (DNL)	DNL			±1	LSB	
Gain error	E_G			±2	LSB	
Offset error	E_{OFFSET}			3	LSB	

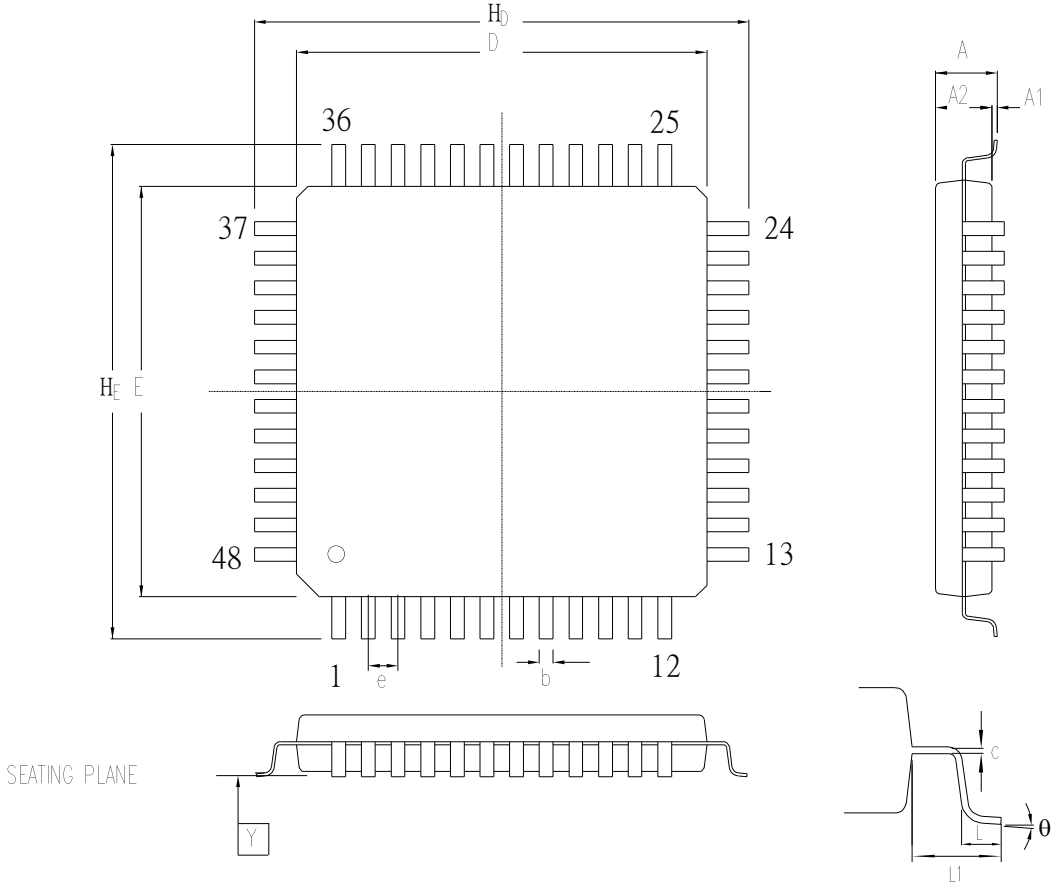
PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Absolute error	E_{ABS}			4	LSB	
ADC Clock frequency	F_{ADC}	5K		6M	Hz	V_{DD} = 5V
Clock cycle	AD_{CYC}	38			Cycle	
Bang-gap voltage	V_{BG}	1.27	1.35	1.44	V	

6.4.6 Flash Memory Characteristics

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Cycling (erase / write) Program memory	N_{CYC}	100			K cycle	
Data retention	T_{RET}	10			years	T_A = +85°C
Erase time of ISP mode	T_{ERASE}	2.3	2.5	2.7	mS	Erase time for one page
Program time of ISP mode	T_{PROG}	57	62	67	μS	Programming time for one word
Program current	I_{PROG}		3.3		mA	V_{DD} = 5.5V

7 PACKAGE DIMENSION

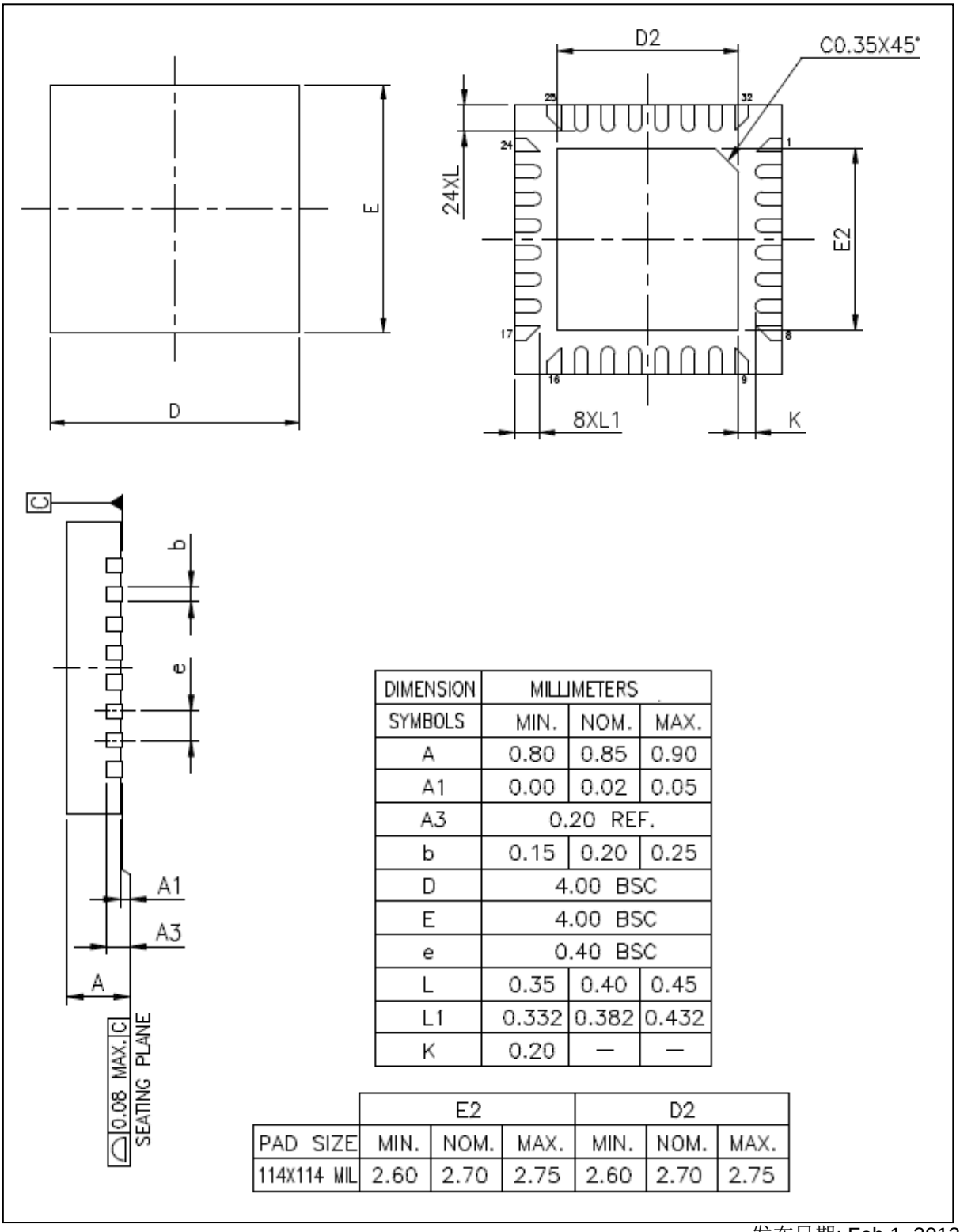
7.1 48-Pin LQFP



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

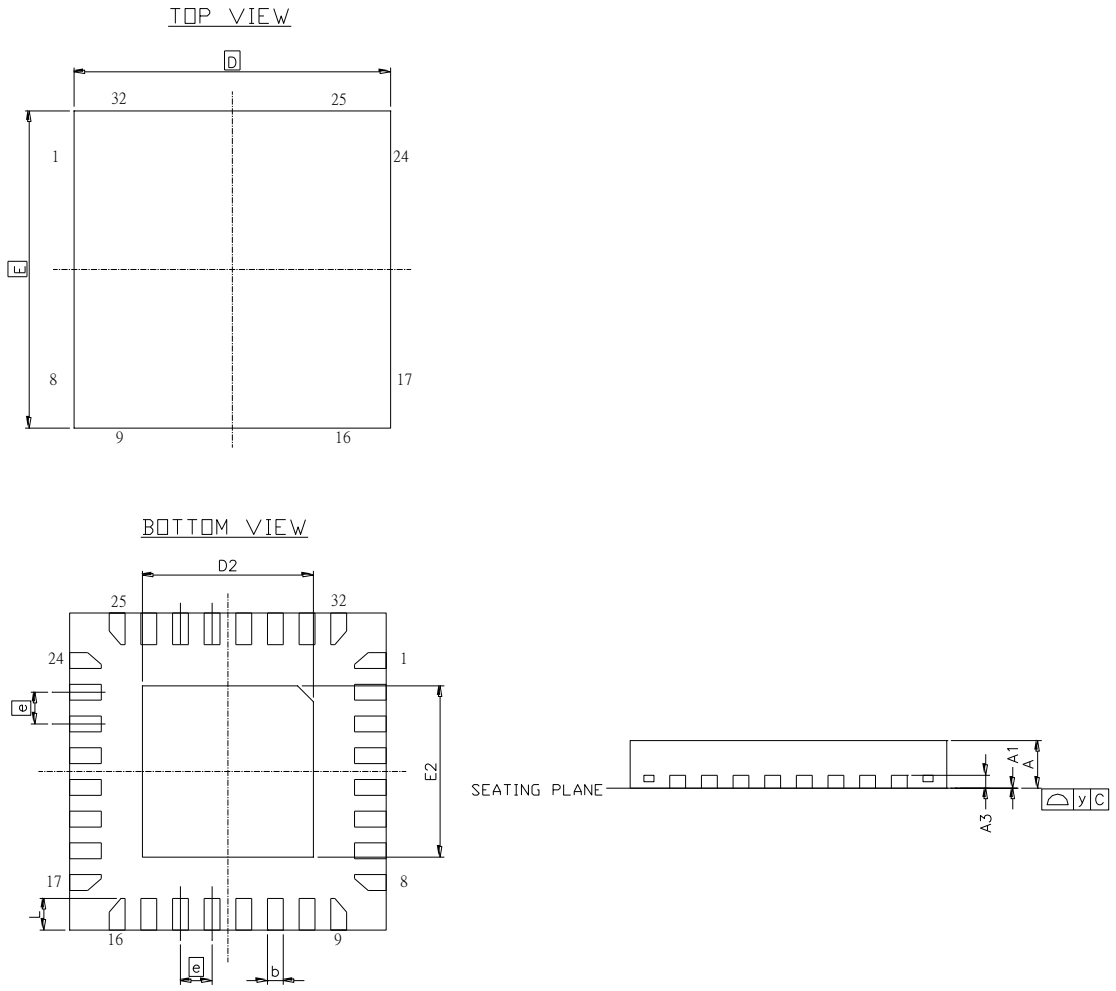
7.2 33-Pin QFN (4mm X 4mm)



DIMENSION	MILLIMETERS		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
L	0.35	0.40	0.45
L1	0.332	0.382	0.432
K	0.20	—	—

	E2			D2		
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
114X114 MIL	2.60	2.70	2.75	2.60	2.70	2.75

7.3 33-Pin QFN (5mm X 5mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
E	5.00 BSC			0.197 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		

SYMBOL	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
DIMENSION (MM)	3.4	3.5	3.6	3.4	3.5	3.6

8 修订历史

日期	修订	修改
Dec 1, 2011	V1.02	Initial release of Chinese version.
Feb 1, 2012	V1.03	1. Add VDD rise rate specification. 2. Revise minimum ADC clock frequency specification. 3. Revise minimum and maximum specification of band-gap voltage. 4. Revise minimum and maximum specification of external input clock. 5. Add flash memory electrical characteristics.

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